International Journal of Latest Engineering Research and Applications (IJLERA) ISSN: 2455-7137

Volume – 02, Issue – 03, March – 2017, PP – 103-109

CONSTRUCTION OF HIGH PERFORMANCE CARRY SKIP ADDER BY APPLYING ADIABATIC LOGIC

Dr. T. Ravichandran [1], P. Kannan [2], V. Singaravelan[3]

[1](DEAN&HOD/ECE, SNS College of technology, Anna University, Coimbatore, India)

[2](ECE, SNS College of technology, Anna University, Coimbatore, India)

[3](ECE, SNS College of technology, Anna University, Coimbatore, India)

Abstract: Adders are of fundamental importance in a wide variety of digital systems. Many fast adders exist, but adding fast using low area and power is still challenging. The most timing critical part of logic design usually contains one or more arithmetic operations, in which addition is commonly involved. In VLSI applications, area, delay and power are the important factors which must be taken into account in the design of a fast adder. A new bit block structure that computes propagate signals called "carry strength" in a skip fashion. Several new adders based on the new carry skip Adder structure are proposed by using adiabatic logic. Comparison with well-known conventional adders demonstrates that the usage of carry-strength signals allows high-speed adders to be realized at significantly lower cost and consuming lower power than previously possible. As well as in this paper we are concentrating on the heat dissipation &we are reducing the current using adiabatic logic. The design of an 8-bit carry-skip adder to achieve minimum power is presented in this paper. The group generates and group propagate functions used in carry look ahead logic is used to speed up multiple stages of carry skip adders. The optimum sizes for the skip blocks are decided by considering the critical path into account. The carry-skip adder reduces the time needed to propagate the carry by skipping over groups of consecutive adder stages, is known to be comparable in speed to the carry look-ahead technique while it uses less logic area and less power. In this paper, a design of 8-bit Carry Skip Adder by various existing logic styles are to be compared quantitatively and qualitatively by performing detailed transistor-level simulation using 180nm technology in cadence virtuoso.

Keywords: carry skip adder, adiabatic logic, less power, less logic area

I. Introduction

A low power VLSI chips become need from such development forces of IC's. In adiabatic logic we used pulsed power supply. In Practically resonant inductor circuits used as power supply. In traditional method Conventional CMOS logic gates used to implement the adders. In charging and discharging produce Dynamic power dissipation. When switching occurs in the transistors (NMOS and PMOS) are conduct current from supply to ground. Recently, adiabatic logic (or energy recovery logic) style has emerged as a promising approaching strong inversion regime, to reduce dynamic power consumption significantly without sacrificing noise immunity and driving ability. These circuits achieve ultralow energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads, especially in low-frequency regime.

Since the performance requirements are quite relaxed in many of this energy efficient sub threshold applications, we believe that the adiabatic style can be used efficaciously in a sub threshold regime to make the circuit more energy efficient. To the best of our knowledge, no paper emphasizes the application of adiabatic logic in weak inversion regime for advanced technology node. To extend battery life, low power operation is desirable in integrated circuits. Furthermore, successive generations of applications often require more computing power, placing greater demands on energy storage elements within the system. Power dissipation limitations come in two flavours. The first is related to cooling considerations when implementing high performance systems. High speed circuits dissipate large amounts of energy in a short amount of time, generating a great deal of heat as a by-product. The adiabatic concepts is inherently taken from mechanical/ thermodynamics engineering which states

"An adiabatic process is one in which no heat is gained or lost by the system". These circuits can be broadly classified as semi/ partial adiabatic and full /complete adiabatic circuits depending upon the level of Follow-nests of the circuit with respect to the principles/ concepts laid down by the adiabatic logic approach.

Hence it is very important to concentrate on low power circuits rather than only high performances circuit, with the advancement of technology in last few years there is a dramatic shift in the approach of the industry researcher to come up with increased functionality and performances. Now the major dissipation in

conventional CMOS circuit can be broadly classified as under two category i.e. static and dynamic power dissipation, which is caused mainly due to the current source, sub threshold MOS current, gate tunnelling, capacitances, involved operation, speed, activity factor etc.

II. ADIABATIC LOGIC DESIGN

The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component.

Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems. Like many other adiabatic logic families, Reversible logic is a dual-rail logic family based upon a pair of cross-coupled inverters that are supplied using a power-clock, rather than a static DC power-supply. The configuration of the evaluation logic is what makes reversible logic an ideal family to implement fully reversible adiabatic logic. This logic is constructed from nMOS devices attached between the power-clock and the outputs.

These nMOS devices take complementary inputs and are constructed to produce a low-resistance path between the power-clock and the asserted output. The non-asserted output should be left with a high-impedance path to power-clock, and will be pulled low by the cross-coupled n-type devices. This means that the function is evaluated when there is sufficient differential between the two outputs, but far more importantly means that by using reverse-flowing data, the outputs can be more completely recovered. This should allow losses to be reduced to leakage.

A. Principle Of Adiabatic Logic

If we reduces the speed of operation we can get very low power dissipation. In adiabatic logic, switching transistors are made of under assured conditions. This adiabatic logic of gates having capacitors here the energies stored and recycled. The recycling is done by using reversing the direction of power supply. So that we can reduces the dissipated heat. So that we can reduces the dissipated heat. So that it is called as energy recovery CMOS. Zero energy loss is impossible, but in adiabatic technique, the circuit energy is conserved, as an alternative of dissipated as heat. This adiabatic technique reduces the power dissipation in digital systems depends on purpose and system needs.

B. Adiabatic Gates

In adiabatic technique first we have to implement standard cell library for SAL logic. Library contains common gates, complex gates, special gates are compulsorily implemented for design basic structure of 8 bit carry skip adder and carry save adder.

In adiabatic logic restructure the conventional gates that is, convention method NAND gate is implemented by 4 gates in adiabatic logic NAND gate is designed by 2 gates as shown in fig.1.

These gates are designed between supply clock and output capacitor. Depending on the context, the term may refer to an ideal logic gate, one that has for instance zero rise time and unlimited fan-out, or it may refer to a non-ideal physical device.

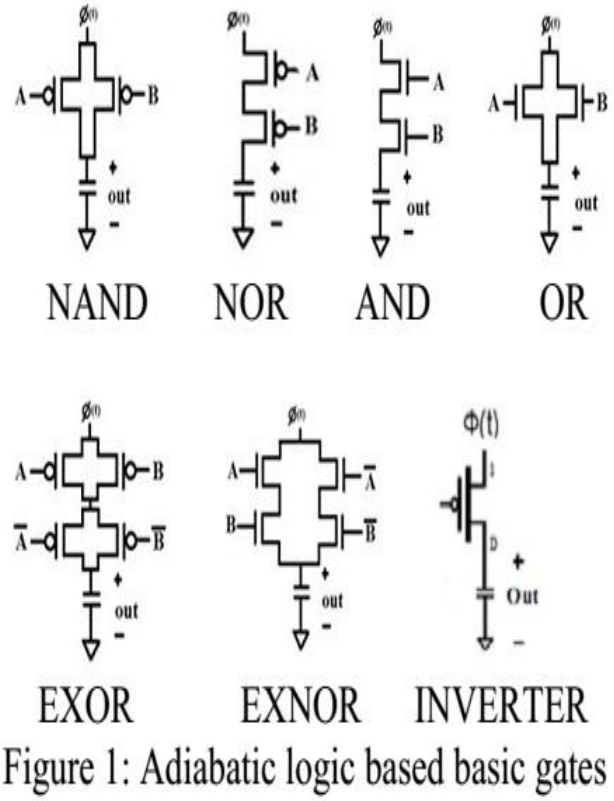


Figure 1: Adiabatic logic based basic gates

Note that all the inputs should also be available in complementary form. Both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle.

To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a pulsed-power supply with the ramped voltage output.

C. Existing Method Adiabatic Logic-Based 4-Bit CLA

In this section, design and analysis of SAL-based 4-bit CLA are given to show the workability and the feasibility of the proposed logics. After verifying the logical functionality, we implemented an SAL-based standard cell library, consisting of common digital gates, such as buffer/inverter, two-input and three-input functions, complex gates, and special gates like half and full adder, which are necessary to implement the 4-bit CLA.

The digital gates of the library are developed at transistor level using ramp type supply voltage as discussed in the previous section. Hence, 22-nm technology file is used in our transistor-level designs which guarantee the manufacturability of our designs under all normal conditions with favourable yields.

In structures of basic logic gates considering SAL are given. These structures resemble either the pull-up or the pull down network of the static conventional logic. For example, to implement a NAND or a NOR gate, simply the pull-up network can be placed between the supply clock and the output load capacitors, whereas an AND or an OR gate can be implemented using the pull-down network between the supply clock and the output load capacitors.

In case of a NAND structure, for every input combination except A = B = 1, the output node voltage will follow the supply clock closely, and we get a triangular output waveform. When A = B = 1 through parallel Pmos transistor, leakage currents will flow as the transistors will behave almost as a constant current source.

A very small amount of charge will be stored across the load capacitor, i.e., instead of ground potential, very small voltage will be dropped across the output. The basic building block of 4-bit CLA is given in Fig. 5.1, which is also very similar to the conventional structure

Hence, we implemented the sum (Si) in three stages to avoid delay mismatching with the carry generation. In SAL-based 4-bit CLA, every stage will be controlled by the supply clock. Like the conventional approach, the expression of the ith sum and the (i + 1)th carry output can be given as

$Si = Ai \oplus Bi \oplus Ci$

$Ci+1 = Ai\ Bi + (Ai \oplus Bi)Ci$

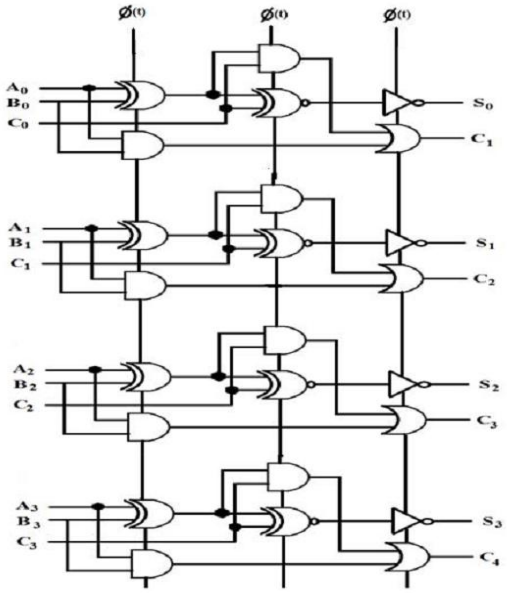
According to the synthesized gate level block, the SAL gate level structure of 4-bit CLA has been implemented using Virtuoso(R) Schematic Composer. In the above explanation of the design which will be easily discussed in the later portion of done in their respective process in their own representation in the proposed system design. Two other important conflicting design parameters are power consumption and speed.

A better metric to indicate the optimal design tradeoffs would be the power delay product or energy consumption per operation. Related to the power consumption is the lowest supply voltage in which the design can still operate properly.

.

III. DESIGN METHODOLOG

The design methodology that should be used when designing a CLA gate is to place the recharge transistor in parallel to the stacked transistors. The stacked transistors will be sized to minimal widths to reduce intrinsic capacitances; increasing dynamic operation performance over reduced static operation performance. This sizing strategy also results in reduced energy dissipation, as compared to conventional static CMOS gates, using adiabatic logic.



IV. PROPOSED METHOD CARRY SKIP ADDER

It is a 8 bit carry skip adder. This adder consists of two blocks one is ripple carry adder block other one is skip chain block. This adder is speeder. In ripple carry adder one full adder input is waiting for another full adder output. So time delay is increased. But in this carry skip chain if the skip chain is detected the 1 means it will automatically skip the operation and it gives the 1 to the next block so it is faster. If no of bits increased this skip adder is most significant.

Thus the given supply voltage is divided in to two parts by using the pMOS and nMOS transistor. Depending on the switching of a transistor in the control circuit the Gate is operated in either full power mode or half power mode. They are carry skip adder designed using adiabatic logic approach as shown in the Figure 6.1.Thus the given supply voltage is divided in to two parts by using the pMOS and nMOS transistor. For adiabatic logic first we have to implement SAL based library. This library consists of logic gates, complex gates, etc. Then using this gates we have to implement digital circuits. In adiabatic logic transistors count approximately half compared to Conventional CMOS logic.

- Comparing to the conventional CMOS logic design method this adiabatic logic transistor count only half.
- The SAL technique can be used to make the circuit have to save energy compared to another method.
- Area is reduced.

- Delay is reduced
- .Reduced heat dissipation.
- Achieved low power so power waste is reduced.

The carry skip adder reduces the delay due to the carry computation. Consider the full-adder's operation. If either input is a logical 1, the cell will propagate the carry input to the carry output. Therefore, the full adder carry input, Ci, will propagate the carry input to its carry output, Ci+1, when Pi = Ai⊕Bi. Multiple full adders, called a block, can generate a "block" propagate signal to detour the incoming carry around to the block's carry output signal. Figure 6.1 shows a 8-bit carry skip adder block.

Each block is a small ripple carry adder producing the block's sum and carry bits. However, each block quickly calculates whether the block's carry input is propagated to its carry output. The carry skip adder provides a compromise between a ripple carry adder and a CLA from the delay due to the propagation of a carry to adder.

The carry skip adder divides the words to be added into blocks. Within each block, ripple carry is used to produce the sum bit and the carry. The Carry Skip Adder reduces the delay due to the carry computation i.e. by skipping over groups of consecutive adder stages [6].

- If each Ai # Bi in a group, then we do not need to compute the new value of Ci+1 for that block; the carry-in of the block can be propagated directly to the next block.
- If Ai = Bi = 1 for some i in the group, a carry is generated which may be propagated up to the output of that group.
- If Ai = Bi = 0, a carry, will not be propagated by that bit location.

The basic idea of a carry-skip adder is to detect if in each group all Ai # Bi and enable the block's carry-in to skip the block when this happens as shown in figure6.1. In general a block-skip delay can be different the next bit position [7][8].

With carry skip adders, the linear growth of carry chain delay with the size of the input operands is improved by allowing carries to skip across blocks of bits, rather than rippling through them.

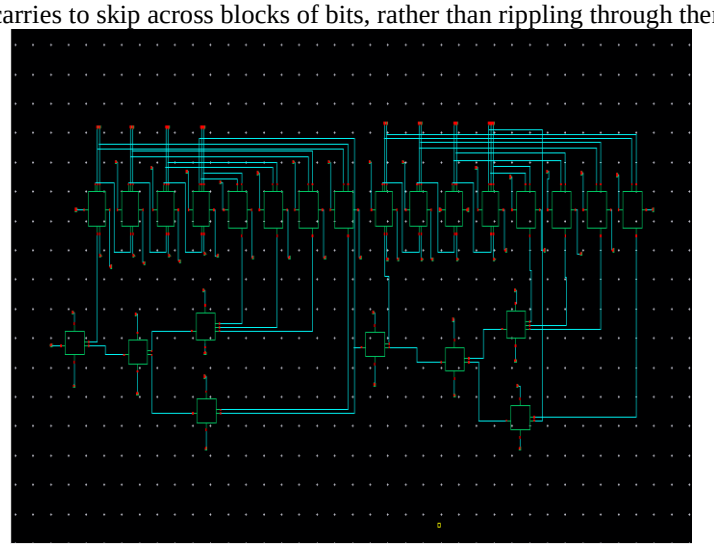


Figure6.1 carry skip adder using adiabatic logic

This is because all the important parameter governing power dissipation-switching capacitance, transition activity, and short-circuit current are strongly influenced by the chosen logic style. Depending on the application, circuit can be implemented in different logic style. Still, other digital logic styles exist and are utilized in the industry as well.

V. SIMULATION AND RESULTS

In order to evaluate the comparative performance of the different 8-bit adders and multipliers, the circuits are implemented in 180nm CMOS technology and simulated at 25 °C using cadence virtuoso tool. The simulation is done with different values of VDD ranging from 1.8V to 3.3 V.

Each topology is analyzed in terms of propagation delay, power dissipation and their product. The propagation delay is measured as the time difference between the instant the input signal reaches 50% of its logic swing and the instant the output also reaches the same value. The power dissipation is evaluated by estimating the power flowing into the circuit. The circuits of four MOS transistors. The input output waveforms of carry skip adder, whereas output power curve . The design has been implemented with the help of 8 transistors which was 4 in case of CMOS design. They make one of the outputs require less logical effort than the other. Some logic designs reduce the logic effort along the critical path by unequal transistor sizes.

This result in varying node capacitance values, and the desired response of the rising/falling outputs is maneuvered, while aiming for reduced power. This asymmetric feature is exploited in the design of Adiabatic Logic.

Time often plays an important role in signal processing systems. Obviously, increasing the clock frequency is one way to improve the throughput, but adiabatic circuits cannot be clocked at very high frequencies. The maximum frequency of operation realized by an adiabatic circuit depends upon the efficiency of the Evaluation and Recovery phases .However, these methods shave sever challenges with the shrink of CMOS technology sizes such as degraded voltage margin, increased leakage currents, and increased soft error rates.

TABLE 7.1 POWER ANALYSIS OF 8-BIT CARRY SKIP ADDER

S.NO	CMOS Circuit	Existing Design-4bit power (µW)	Proposed Design-4bit power (µW)	Proposed design-8bit power (µW)
1	NOT Gate	28.84	15.31	13.46
2	AND Gate	12.44	6.45	6.21
3	OR Gate	17.21	9.310	9.11
4	NAND Gate	10.59	5.630	5.22
5	NOR Gate	10.43	6.151	6.03
6	EX-OR Gate	34.50	18.34	18.40
7	Full Adder	1215	79.81	78.56
8	CLA Adder	915.30	66.79	67.69
9	CSK Adder	19950	13170	10650

S.NO	CMOS Circuit	Existing Design-4bit Delay (PS)	Proposed Design-4bit Delay (PS)	Proposed design-8bit Delay (PS)
1	NOT Gate	26.56	25.98	26.02
2	AND Gate	20.06	20.06	20.06
3	OR Gate	40.01	39.21	39.85
4	NAND Gate	20.05	20.05	20.05
5	NOR Gate	49.41	47.77	48.42
6	EX-OR Gate	65.15	65.23	65.27
7	Full Adder	140.30	140.25	141.60
8	CLA Adder	142.90	142.79	142.88
9	CSK Adder	599.70	598.99	594.20

For each value of supply voltage, we first performed the functional frication for each topology considering all possible input transitions. Comparison analysis of an 8-bit adder design and 8-bit multiplier design is depicted in Table 7.1.

It is apparent that Carry skip adder architecture has smaller delays, even though its speed advantage is greatly reduced for lower VDD. At high supply voltages Carry skip adder are always faster than the earlier version. At VDD = 3.3 V, propagation delay of Carry skip adder is 29.21% less than carry look ahead adder and 6.09% less than adder but it consumes more power in comparison with the other two adder designs.

Table7.2 DELAY ANALYSIS OF 8-BIT CARRY SKIP ADDER depicts that adiabatic logic involving carry skip adder have the lowest delay as compared with other multiplier architectures. Eight-bit multiplier design using multi output CLA adder has 26.39% less delay than the multiplier with CMOS full adder and 13% improvement in delay as compared to multiplier designed using DPL adder at VDD = 3.3 V. Due to large number of transistors in CLA adder the power consumption of CLA adder is more than both CMOS and adder structures. At VDD= 3.3V carry skip adder delay is 49.41% more than CMOS and 7.5% more than multiplier with CLA adder.

VI. CONCLUSION AND FUTURE WORK

A. Conclusion

Thus the carry skip adder is designed using the design-1 and design-2 approach adiabatic logic method. These gates are used as building blocks for the development of the adiabatic logic carry skip adder circuits in order to reduce the power consumption and also the leakage current. The power consumed by the sub clock circuit is only about 46% when comparing to the ideal circuit. Similarly the energy consumed by the circuit is also reduced up to 40% compare to the existing/ideal circuits. This method is does not affect the performance of the circuit, delay of the circuit is similar to that of the ideal CMOS circuit and produce about 95% of efficiency.

This can be implemented in any kind of logic in digital circuit. These designs can be extended to dual sleep technique and also in dual stack technique in order to utilize the whole circuit performance. Sub clocking is the technique which is more efficient than that of the adiabatic logic and ideal circuit without sub clock method. Depending on the technology (180nm) and period of operation the energy consumption can be vary and also the power consumption is reduced up to 54%. To get the proper operating point the width of the transistor is varied using the Cadence Virtuoso tool.

B. Future Work

In later works the project is implemented in various technologies and also in various circuits in order to obtain a minimum power. Depending on the number of transaction the power consumption also varies thus the circuit is tuned with different width range and power is calculated. Result of this process is to determine the minimum operating voltage level of the circuit and also calculating the power consumption.

References

[1]. ManashChanda, Sankalp Jain, Swapnadip De, Chandan Kumar Sarkar,"Implementation of Subthreshold Adiabatic Logic for Ultralow-Power Application, "IEEE transactions on very large scale integration (vlsi) systems", 2015.*)*

[2]. S.Soundarya, M.S.Anusooya, V.JeanShilpa PG student, VLSI and Embedded systems,Assistant professor of ECE Dept. B.S. Abdurrahman university, Chennai, Design And Analysis Of Low Power Adders Using Subthreshold Adiabatic Logic,",VOLUME-3,ISSUE-3,2016. I. S. Jacobs and C. P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.

[3]. A.Calimera, A. Macii, E. Macii, and M. Poncino, "Design techniques and architectures for low-leakage SRAMs,"IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 9, pp. 1992–2007, Sep. 2012.

[4]. J. Kwong, Y. K. Ramadass, N. Verma, and A. P. Chandrakasan, "A 65 nm sub-Vt microcontroller with integrated SRAM and switched capacitor DC-DC converter," IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 115–126, Jan. 2009.

[5]. C.-S. A. Gong, M.-T. Shiue, C.-T.Hong and K.-W.Yao, "Analysis and design of an efficient irreversible energy recovery logic in 0.18-μm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 9, pp. 2595–2607, Oct. 2008.

[6]. B. H. Calhoun and A. P. Chandrakasan, "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS," IEEE J. Solid-State Circuits, vol. 41, no. 7, pp. 1673–1679, Jul. 2006.

[7]. S. Hanson, M. Seok, D. Sylvester, and D. Blaauw,"Nanometer device scaling in subthreshold logic and SRAM," IEEE Trans. Electron Devices, vol. 55, no. 1, pp. 175–185, Jan. 2008.

[8]. T.-T. Liu and J. M. Rabaey, "A 0.25 V 460 nW asynchronous neural signal processor with inherent leakage suppression," IEEE J. Solid-State Circuits, vol. 48, no. 4, pp. 897–906, Apr. 2013

