Low-Power High-Speed Circuit Design for VLSI Memory Systems under Recent Techniques

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Abstract: In current PC systems, different memory parts are utilized, for example, on-chip enlist documents, on-chip/off-chip reserve recollections, and off-chip primary recollections. High-speed memory framework design has been and will have been a standout amongst the most imperative issues. In microchips, for instance, the on-chip reserve sizes are developing with every era to connect the expanding disparity in the speeds of the processor and the principle memory. Power dissemination has likewise turned into a vital thought both because of the expanded reconciliation and working speeds, and in addition because of the unstable development of battery worked machines. In the theory, low-power high-speed circuits for recollections and processor-memory interface are researched.

To start with, anomalous spillage concealment (ALS) plan is proposed to repair standby current blunders in SRAMs because of gadget imperfections. By presenting spillage sensors, move registers and breakers the ALS faculties 1µA of irregular spillage, detaches the memory cell deliberately from VDD lines and along these lines smothers strange spillage current. A 64Kbit test SRAM is created in 0.6µm CMOS innovation and the viability are illustrated. The range overhead reductions with the development of memory limit, and turn out to be under 1% for 4Mbit SRAMs, which guarantee the commonsense utilization of this plan in business applications.

Keywords: ALS, ISSCC, MTCMOS, VTCMOS, RRDV, PMOSRRDV, NMOSRRDV

I. Introduction

In modern computer systems, hierarchical memory architecture is widely used. There are various memory components inside one system, such as register files, cache memories, and main memories. High-speed memory system design has been and will have been one of the most important design issues. As systems go toward higher performance, capacity of these memories gets larger. In microprocessors, for example, on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. Power dissipation has also become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. Figure 1.1 shows power trend of MPUs and DSPs presented at International Solid-State Circuits Conference (ISSCC) [1]. Power consumption of high-end processors is now over 100W. Today, low power is not only an issue for portable applications but also a stringent demand for high-speed applications.
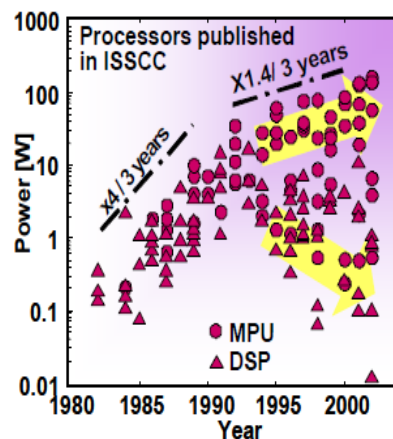

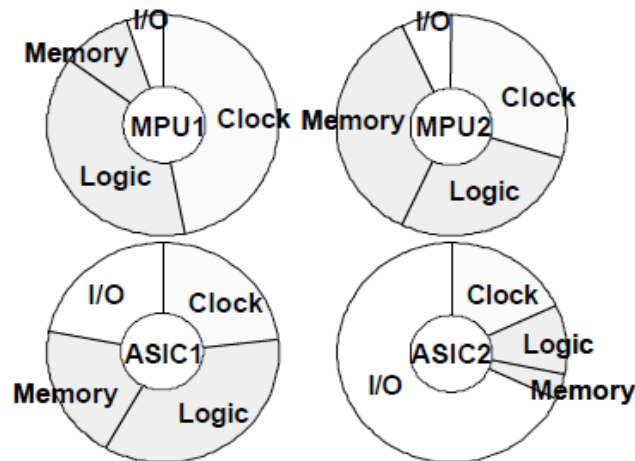Figure 1.1: Power trend of MPUs and DSPs presented ISSCC.

Figure 1.2: Power Distribution in CMOS LSIs.

Fig 1.1 shows several important parameters of future high-performance LSIs predicted by SIA [2]. In the year 2016, when the mainstream technology is shrunk down to 22nm gate length, the maximum on-chip clock frequency is 29GHz, microprocessor power is 288W with 0.5V supply voltage, and number of I/O pins is 7100. These goals cannot be reached by simply taking advantage of scaling scenario [3], since scaling of I/O related circuits is slower than that of core logic circuits. The main reasons lie in difficulties of packaging and also in special design considerations regarding me /Os such as ESD protection.

II. Classification of Power Consumption

Though there are different types of power consumption, the major types that affect CMOS circuits are dynamic power and leakage power [1].

2.1. Dynamic power

Dynamic power [2] is the power that is consumed by a device when it is actively switching from one state to another [3]. Dynamic power consists of switching power consumed while charging and discharging the loads on a device, and internal power (also referred to as short circuit power), consumed internal to the device while it is changing state [4]. Fig. 1 shows the dynamic power dissipation that can occur in CMOS circuits.
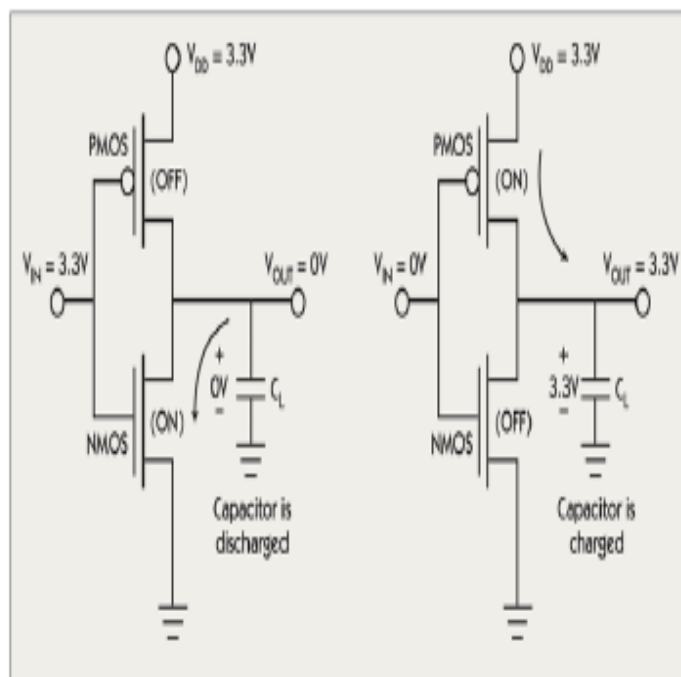
III. Adaptive Techniques

The power and the delay dependence on the threshold voltage at 0.5 *VDD* is shown in Fig. From Fig., it is inferred that to achieve high performance, *Vth* has to be decreased. But decreasing *Vth* could cause a significant increase in static leakage power component.
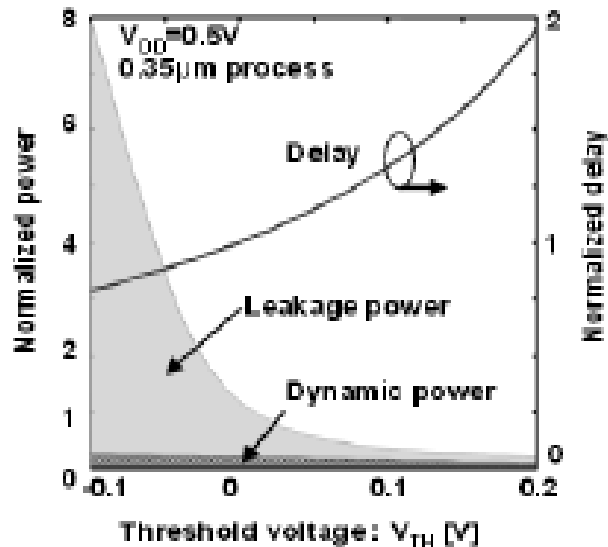
There are several approaches to reduce the stand by leakage current like MTCMOS (Multi Threshold CMOS) and VTCMOS (Variable Threshold CMOS) [11]. These schemes cannot suppress the active leakage power. Another approach is a dual threshold voltage approach, which is to partition a circuit into critical and non critical gates and use low *Vth* transistors only in the critical gates. The drawback of this scheme is that the leakage current cannot be sufficiently suppressed since the large leakage current always flows through the low *Vth* transistors.

1) Vth Hopping

Dynamic threshold voltage hopping scheme solves these problems [15]. This scheme utilizes dynamic adjustment of frequency and *Vth* through back gate bias control depending on the workload of the processor. When the workload is decreased, less power would be consumed by increasing *Vth* as depicted in Fig. This approach is similar to the dynamic *VDD* scaling, DVS. In the DVS scheme, voltage and frequency are controlled dynamically based on the workload variation.

IV. Conclusion

In this paper, circuit designs for future low-power high-speed memory systems are proposed. Fundamental memory circuit designs are explained especially on SRAMs and register files. Abnormal leakage suppression scheme is proposed to repair standby current errors in SRAMs. By introducing leakage sensors, shift registers and fuses the ALS senses 1μA of abnormal leakage, isolates the memory cell systematically from VDD lines and thus suppresses abnormal leakage current. A 64Kbit test SRAM is fabricated in 0.6μm CMOS technology and the effectiveness are demonstrated. The area overhead decreases with the growth of memory capacity, and becomes less than 1% for 4Mbit SRAMs, which assures the practical use of the scheme.

Dual VDD and dual VTH memory designs including an SRAM and a register file is presented. High speed level-up converter using pseudo NMOS topology can reduce conversion delay to 50% of conventional circuits. A test chip integrating several level converters is designed in 0.6μm CMOS technology and measured. The level converter is modified with replica adaptive bias circuits and implemented in a dual VDD SRAM and a register file. A test chip is fabricated in 0.25μm triple- metal FD SOI CMOS technology. 2K-bit SRAMs and a 256-bit register file are integrated on a 16-bit microprocessor. The measured performance of the SRAM is 400MHz at 0.5/1.0V, 800MHz at 0.9V/1.8V, and 180MHz at 0.5V/0.5V supply voltage.

Fine-grain leakage control method is introduced and row-by-row dynamic VDD (RRDV) control scheme is proposed to suppress leakage power of dormant cells in an active mode. Cell leakage is reduced through DIBL effects when cell VDD of un-accessed rows is lowered to 0.2VDD, while bit- line leakage is reduced by applying negative voltage on inactive word lines. Measurement and simulation results indicate that

the RRDV scheme can achieve 99.9% leakage reduction in scaled devices. The delay and area overhead of the RRDV scheme is estimated to be 5% and less than 7% respectively. Two variation of RRDV scheme, PMOS RRDV and NMOS RRDV are presented and their tradeoffs are discussed. PMOS RRDV controls cell data swing from VDD side while NMOS RRDV controls from VSS side. In terms of delay, area overhead, and noise margin, PMOS RRDV is superior to NMOS RRDV.

Sense amplifying cell (SAC) scheme to reduce 90% write power in wide SRAMs is also proposed in Chapter 5. SAC uses low-swing write technique with a 7-transistor cell. A test chip is fabricated in 0.35µm CMOS technology and the effectiveness is demonstrated through measurements. It is pointed out that by combining SAC and NMOS RRDV scheme, reducing both leakage and write power is possible without using negative word line, which is great advantage of NMOS RRDV over PMOS RRDV.

A low-power yet high-speed memory-to-processor interface scheme, Wireless Super connects (WSC) scheme is proposed with the density of 625 pins/mm2. The interface utilizes capacitive coupled contact- less mini-pads, return-to- half-VDD signaling and sense amplifying F/F. The measured test chip in 0.35µm CMOS delivers up to 1.27 Gbps/pin with the power consumption of 3mW/pin. SPICE simulations with predicted 70nm transistor model shows that 7000 I/O's can be operate at 8.0GHz with only 1.63W.

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